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6296104, B1999-08-1265B-054, C1999-08-5210B-037; 19990701.

**Title**

Equivalence checking of combinational circuits using Boolean expression diagrams.

**Author(s)**[Hulgaard-H;](#) [Williams-P-F;](#) [Andersen-H-R.](#)**Author affiliation**

Dept of Inf Technol, Tech Univ, Lyngby, Denmark.

**Source**

IEEE-Transactions-on-Computer-Aided-Design-of-Integrated-Circuits-and-Systems (USA), vol.18, no.7, p.903-17, July 1999. , Published: IEEE.

**CODEN**

ITCSDI.

**ISSN**

ISSN: 0278-0070, CCCC: 0278-0070/99/ (\$10.00)..

**Availability**

SICI: 0278-0070(199907)18:7L.903:ECCC; 1-N

Electronic Journal Document Number: S0278-0070(99)05031-9.

**Publication year**

1999.

**Language**

EN.

**Publication type**

J Journal Paper.

**Treatment codes**

P Practical; T Theoretical or Mathematical; X Experimental.

**Abstract**

The combinational logic-level equivalence problem is to determine whether two given combinational circuits implement the same Boolean function. This problem arises in a number of computer-aided design (CAD) applications, for example when checking the correctness of incremental design changes (performed either manually or by a design automation tool). This paper introduces a data structure called Boolean expression diagrams (BEDs) and two algorithms for transforming a BED into a reduced ordered binary decision diagram (OBDD). BEDs are capable of representing any Boolean circuit in linear

space and can exploit structural similarities between the two circuits that are compared. These properties make BEDs suitable for verifying the equivalence of combinational circuits. BEDs can be seen as an intermediate representation between circuits (which are compact) and OBDD's (which are canonical). Based on a large number of combinational circuits, we demonstrate that BEDs either outperform or achieve results comparable to both standard OBDD approaches and the techniques specifically developed to exploit structural similarities for efficiently solving the equivalence problem. Due to the simplicity and generality of BEDs, it is to be expected that combining them with other approaches to equivalence checking will be both straightforward and beneficial. (46 refs).

**Descriptors**

binary-decision-diagrams; Boolean-functions; circuit-CAD;  
combinational-circuits; data-structures; logic-CAD.

**Keywords**

equivalence checking; combinational circuits; Boolean expression diagrams; CAD applications; incremental design changes; design automation tool; data structure; BED; reduced ordered binary decision diagram; linear space; structural similarities.

**Classification codes**

B1265B	(Logic circuits).
B1265A	(Digital circuit design, modelling and testing).
B1130B	(Computer-aided circuit analysis and design).
B0250	(Combinatorial mathematics).
C5210B	(Computer-aided logic design).
C4230B	(Combinatorial switching theory).
C5120	(Logic and switching circuits).
C7410D	(Electronic engineering computing).
C1160	(Combinatorial mathematics).

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### Accession number & update

6615178, C2000-07-4210-046; 20000601.

### Title

Difference decision diagrams.

### Author(s)

[Moller-J](#); [Lichtenberg-J](#); [Andersen-H-R](#); [Hulgaard-H](#); Ed. by [Flum-J](#); [Rodriguez-Artalejo-M](#).

### Author affiliation

IT Univ in Copenhagen, Denmark.

### Source

Proceedings of CSL'99: Annual Conference of the European Association for Computer Science Logic, Madrid, Spain, 20-25 Sept. 1999.

Sponsors: Comision Interministerial de Ciencia y Tecnologia, Dept. Arquitectura de Computadores y Automatica, et al.

In: p.111-25, 1999.

### ISSN

ISBN: 3-540-66536-6.

### Publication year

1999.

### Language

EN.

### Publication type

CPP Conference Paper.

### Treatment codes

T Theoretical or Mathematical; X Experimental.

### Abstract

This paper describes a new data structure, difference decision diagrams (DDD), for representing a Boolean logic over inequalities of the form  $x-y \leq c$  where the variables are integer or real-valued. We give algorithms for manipulating DDD and for determining validity, satisfiability, and equivalence. DDD enable an efficient verification of timed systems modeled as, for example, timed automata or timed Petri nets, since both the states and their associated timing information are represented symbolically, similar to how BDD represent Boolean predicates. We demonstrate the efficiency of DDD by analyzing a timed system and compare the results with the tools KRONOS and UPPAAL. (28 refs).

### Descriptors

[automata-theory](#); [Boolean-functions](#); [computability](#); [data-structures](#);  
[decision-diagrams](#); [formal-verification](#); [Petri-nets](#); [real-time-systems](#).

### Keywords

difference decision diagrams; data structure; Boolean logic; integer variables; real valued variables; validity; satisfiability; equivalence; timed systems; timed automata; timed Petri nets; KRONOS; UPPAAL.

**Classification codes**

C4210 (Formal logic).  
C1160 (Combinatorial mathematics).  
C6110F (Formal methods).  
C6120 (File organisation).

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5658864, C9709-4210-093; 970805.

**Title**

Boolean expression diagrams.

**Author(s)**[Andersen-H-R](#); [Hulgaard-H](#).**Author affiliation**

Dept of Inf Technol, Tech Univ, Lyngby, Denmark.

**Source**

Proceedings of Twelfth Annual IEEE Symposium on Logic in Computer Science, Warsaw, Poland, 29 June-2 July 1997.

Sponsors: IEEE Tech. Committee on Math. Found. Comput., IEEE Comput. Soc., SIGACT ACM, Assoc. Symbolic LogicEur. Assoc. Theoretical Comput. SciBRICS, Univ. AarhusInst. Inf., Warsaw UnivPolish Acad. Sci.: Math. Inst. & Committee for MathPolish-Japanese Inst. Comput. TechPolish Minist. EducSun Microsystems., PolandUS Office of Naval ResWroclaw Univ.  
In: p.88-98, 1997.

**ISSN**

ISBN: 0-8186-7925-5, CCCC: 1043-6871/97/ (\$10.00).

**Publication year**

1997.

**Language**

EN.

**Publication type**

CPP Conference Paper.

**Treatment codes**

T Theoretical or Mathematical.

**Abstract**

This paper presents a new data structure called Boolean Expression Diagrams (BEDs) for representing and manipulating Boolean functions. BEDs are a generalization of Binary Decision Diagrams (BDDs) which can represent any Boolean circuit in linear space and still maintain many of the desirable properties of BDDs. Two algorithms are described for transforming a BED into a reduced ordered BDD. One closely mimics the BDD apply-operator while the other can exploit the structural information of the Boolean expression. The efficacy of the BED representation is demonstrated by verifying that the redundant and non-redundant versions of the ISCAS 85 benchmark circuits are identical. In particular, it is verified that the two 16-bit multiplication circuits (c6288 and c6288nr) implement the same Boolean functions. Using BEDs, this verification problem is solved in less than a second, while using

standard BDD techniques this problem is infeasible. BEDs are useful in applications where the end-result as a reduced ordered BDD is small, for example for tautology checking. (23 refs).

**Descriptors**

Boolean-functions; data-structures; decision-tables.

**Keywords**

data structure; Boolean Expression Diagrams; Boolean functions; Binary Decision Diagrams; reduced ordered; tautology checking.

**Classification codes**

C4210 (Formal logic).

C4230 (Switching theory).

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[PDF] [FAST BACKTRACK-FREE PRODUCT CONFIGURATION USING A PRECOMPILED ...](#)

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We can think of **product configuration** as a process of specifying a **product ... (BDD)** is a rooted **directed acyclic graph** representing a Boolean function on a ...

[www.productmodels.org/conference2004/papers/PETO30\\_Hadzic.pdf](http://www.productmodels.org/conference2004/papers/PETO30_Hadzic.pdf) -

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... the demand for the increased needs for customization lead to **product configuration ...**

Definition 3: A ROBDD is rooted, **directed acyclic graph** with... ..

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[PDF] [Integrating CSP Decomposition Techniques and BDDs for Compiling ...](#)

File Format: PDF/Adobe Acrobat - [View as HTML](#)

CSP are equivalent to valid **configurations** of the corresponding **product** model. ... standard shortest path algorithm for **directed acyclic graphs** [26]. ...

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User provided **product configurations** are identified and memorized along with ... system when compositing images represented as a **directed acyclic graph**. ...

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**configuration** of the undirected edges in an essential **graph ...** labeled essential **directed acyclic graphs**, Discrete Math. (submitted, 2000). ...

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[PDF] [The Size Distribution for Markov Equivalence Classes of Acyclic ...](#)

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digraphs or ADGs (also called **directed acyclic graphs** or dags), ... **configuration** of the undirected edges in an essential **graph** dictates the size of the ...

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diverse and include ordinary **product configuration** as well as sales ... (BDD) is a rooted **directed acyclic graph** representing a Boolean function on a ...

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[PDF] [Efficient Assembly of Product Structures in Worldwide Distributed ...](#)

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**configure product** instances. A user can choose some, all or none of these ... Partitioning **directed acyclic** condition **graphs** seems to be similar to the ...

[www.informatik.uni-ulm.de/dbis/01/dbis/downloads/MDF03.pdf](http://www.informatik.uni-ulm.de/dbis/01/dbis/downloads/MDF03.pdf) - [Similar pages](#)

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The **configuration** management data on a **product** generated by one tool cannot be used by ... **directed acyclic graph**, as shown in Figure 2, which is ...

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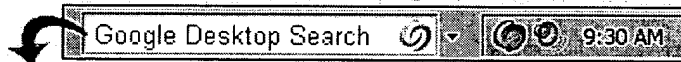
sum-product algorithm, which operates in a factor **graph** and at- ... random fields) and models based on **directed acyclic graphs**. (Bayesian networks). ...

[www.eecs.berkeley.edu/~dolecek/coding/LoeligerFactorGraphs.pdf](http://www.eecs.berkeley.edu/~dolecek/coding/LoeligerFactorGraphs.pdf) - [Similar pages](#)

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## Inventor Information for 09/996745

Inventor Name	City	State/Country
✓ LICHTENBERG, JAKOB	CHARLOTTENLUND	DENMARK
✓ ANDERSEN, HENRIK REIF	BAGSVAERD	DENMARK
✓ HULGAARD, HENRIK	COPENHAGEN	DENMARK
✓ MOLLER, JESPER	COPENHAGEN	DENMARK
RASMUSSEN, ANDERS STEEN	LYNGBY	DENMARK

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## Inventor Name Search Result

Your Search was:

Last Name = RASMUSSEN

First Name = ANDERS

Application#	Patent#	Status	Date Filed	Title	Inventor Name 2
<a href="#">60251862</a>	Not Issued	159	12/08/2000	VIRTUAL TABULATION	RASMUSSEN, ANDERS STEEN
<a href="#">09996745</a>	Not Issued	030	11/30/2001	METHOD OF CONFIGURING A PRODUCT	RASMUSSEN, ANDERS STEEN

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**Inventor Name Search Result**

Your Search was:

Last Name = MOLLER

First Name = JESPER

Application#	Patent#	Status	Date Filed	Title	Inventor Name 2
<a href="#">09996745</a>	Not Issued	030	11/30/2001	METHOD OF CONFIGURING A PRODUCT	MOLLER, JESPER
<a href="#">09763753</a>	Not Issued	041	04/27/2001	DATA STRUCTURE AND ITS USE	MOLLER, JESPER

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**PALM INTRANET**Day : Friday  
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Time: 13:46:03**Inventor Name Search Result**

Your Search was:

Last Name = HULGAARD

First Name = HENRIK

Application#	Patent#	Status	Date Filed	Title	Inventor Name 4
<a href="#">60251862</a>	Not Issued	159	12/08/2000	VIRTUAL TABULATION	HULGAARD, HENRIK
<a href="#">09996745</a>	Not Issued	030	11/30/2001	METHOD OF CONFIGURING A PRODUCT	HULGAARD, HENRIK
<a href="#">09763753</a>	Not Issued	041	04/27/2001	DATA STRUCTURE AND ITS USE	HULGAARD, HENRIK
<a href="#">09116835</a>	<a href="#">6408262</a>	150	07/17/1998	METHOD AND AN APPARATUS FOR ANALYZING A STATE BASED SYSTEM MODEL	HULGAARD, HENRIK

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**Inventor Name Search Result**

Your Search was:

Last Name = ANDERSEN

First Name = HENRIK

Application#	Patent#	Status	Date Filed	Title	Inventor Name 50
<a href="#">60424339</a>	Not Issued	159	11/07/2002	INCHWORM MECHANISM	ANDERSEN, HENRIK
<a href="#">60331018</a>	Not Issued	159	11/06/2001	INCHWORM MECHANISM	ANDERSEN, HENRIK
<a href="#">60301837</a>	Not Issued	159	07/02/2001	FLEXIBLE TOOL FOR HANDLING SMALL OBJECTS	ANDERSEN, HENRIK
<a href="#">60251862</a>	Not Issued	159	12/08/2000	VIRTUAL TABULATION	ANDERSEN, HENRIK REIF
<a href="#">60200029</a>	Not Issued	159	04/26/2000	ANKLE-FOOT ORTHOSIS AND A METHOD FOR MAKING THE SAME	ANDERSEN, HENRIK S.
<a href="#">60148564</a>	Not Issued	159	08/13/1999	A CONVEYOR AND A METHOD FOR CONVEYING ARTICLES ALONG A CONVEYOR	ANDERSEN, HENRIK
<a href="#">60119036</a>	Not Issued	159	02/08/1999	ENHANCEMENT OF BEVERAGE SHELF-LIFE WITH D-TAGATOSE	ANDERSEN, HENRIK
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<a href="#">60075694</a>	Not Issued	159	02/24/1998	PREBIOTIC COMPOSITION	ANDERSEN, HENRIK
<a href="#">60070480</a>	Not Issued	159	01/05/1998	COMBINATION OF D-TAGATOSE AND A SWEETENER	ANDERSEN, HENRIK
<a href="#">60054858</a>	Not Issued	159	08/06/1997	TILTABLE NUT	ANDERSEN, HENRIK
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				SURFACE PROCESSES	
<u>10511462</u>	Not Issued	020	04/11/2005	METHOD FOR MEASURING CURRENTS IN A MOTOR CONTROLLER AND MOTOR CONTROLLER USING SUCH METHOD	ANDERSEN, HENRIK ROSENDAL
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<u>10472213</u>	Not Issued	030	10/15/2003	APPARATUS FOR FLUSHING PERIPHERAL ORGANS IN HUMANS OR ANIMALS	ANDERSEN, HENRIK
<u>10462753</u>	Not Issued	061	06/17/2003	CONVEYOR/SORTER SYSTEM, A LOADING CONVEYOR AND A CONTROL SYSTEM FOR SUCH CONVEYORS	ANDERSEN, HENRIK
<u>10183559</u>	<u>6741912</u>	150	06/28/2002	FLEXIBLE TOOL FOR HANDLING SMALL OBJECTS	ANDERSEN, HENRIK
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<u>09116835</u>	<u>6408262</u>	150	07/17/1998	METHOD AND AN APPARATUS FOR ANALYZING A STATE BASED SYSTEM MODEL	ANDERSEN, HENRIK REIF
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<u>08863746</u>	<u>5846968</u>	150	05/27/1997	N-SUBSTITUTED AZAHETEROCYCLIC CARBOXYLIC ACIDS AND ESTERS	ANDERSEN, HENRIK S.
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<u>08638086</u>	<u>5773943</u>	250	04/25/1996	DRIVE DEVICE FOR A REVOLVING DOOR	ANDERSEN, HENRIK
<u>08627750</u>	<u>5827856</u>	250	04/02/1996	A METHOD OF TREATING INSULIN RESISTANCE	ANDERSEN, HENRIK S.
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<u>08623807</u>	<u>5698551</u>	150	03/29/1996	NOVEL HETEROCYCLIC COMPOUNDS	ANDERSEN, HENRIK S.
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<u>08544682</u>	<u>5795888</u>	150	10/18/1995	N-SUBSTITUTED AZAHETEROCYCLIC CARBOXYLIC ACIDS AND ESTERS THEREOF	ANDERSEN, HENRIK
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<a href="#">07496129</a>	Not Issued	161	03/19/1990	DNA SEQUENCE	ANDERSEN, HENRIK D.
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<a href="#">06060411</a>	<a href="#">4247773</a>	150	07/25/1979	METHOD FOR QUANTITATIVELY DETERMINING FAT IN A FAT-CONTAINING SAMPLE	ANDERSEN, HENRIK R.

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<a href="#">09996745</a>	Not Issued	030	11/30/2001	METHOD OF CONFIGURING A PRODUCT	LICHTENBERG, JAKOB
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09996745Claims Priority from Provisional Application 60251862

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